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Modification of Dynamic Logic Circuit Design Technique for Minimizing Leakage Current and Propagation Delay

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***Abstract*—This paper is based on the OR logic operation's small discharging current and transmission time delay dynamic logic circuit configuration method. In terms of static logic circuits, it require a larger number of transistors and consume a massive amount of power. However, high-speed dynamic logic circuits consume less power due to their lower number of transistors. But, it has an issue with the evaluation phase where current gets leaked from the dynamic node due to sub-threshold leakage. In this paper, we have shown a new dynamic logic circuit design procedure for reducing leakage current from the dynamic node by using delay component, stacking effect, current mirror circuit with footed nmos, and a keeper circuit with the keeper device. The suggested system is analyzed in LTSpice with 45nm CMOS predictive technology model and compared with the previous research to demonstrate validity. The simulation study demonstrates power savings relative to traditional architecture and verifies the suggested strategy. This circuit could be used for designing low power consuming and delay systems for wide fan-in and can be useful for cascading several stages.**

***Index Terms*—leakage current, propagation delay, evaluation period, domino logic, PDN, delay circuit, Stacking effect, keeper circuit, mirror circuit.**

I. Introduction

In CMOS circuits, logic functions are achieved by switching the current flow channels of MOSFETs. The most common CMOS circuits are static logic gates because they are simple to construct, have controlled features, and have a high noise immunity [1]. The fundamental framework for static logic is provided by the CMOS inverter. A full-rail output voltage swing and completely dynamic power dissipation are produced when nMOS and pMOS transistors are used in complementary fashion. Whereas, clocked pMOS pullup is used by dynamic gates. Precharge and Evaluate are the two modes of operation used to create the logic function or logic gate. Here, fewer transistors (N+2) are needed than in static CMOS circuits (2N), yet the circuit still requires less transistors per ratio than static [2] [3].

Fig. 1 is a 4-bit basic dynamic logic circuit with an OR logic operation. At the PUN(pull up network), only a pmos Mp is connected with the clock for getting evaluation and precharge phase. And its source is connected to a power supply voltage (Vdd). After this precharge device, the drain terminal is called dynamic node. A nmos M5 and a PDN (pull down network) and the dynamic node are linked beneath it. In PDN, all the input gates are labeled and all are in parallel connection because an OR logic operation is performed. In the dynamic node, a not gate is connected to form a domino logic circuit for the required output and cascading several stages [4].
When the clock is in a logic low state, known as the precharge phase, the dynamic node is charged up to supply voltage.While the evaluation phase is when the clock is in a logic high state, when the dynamic node is not being charged through the precharge device. If any PDN of the OR logic gate input is in a logic high state during evaluation then the pull-down network and ground are used to discharge the dynamic node. Otherwise, the dynamic node should preserve the voltage up to vdd when the evaluation phase occurs. However, this does not always occur. In the pull down network, transistors have some subthreshold leakage current [5]. As a result, if the pull down network is turned off during the evaluation phase, the dynamic node is gradually discharged into the PDN. That's a problem for the dynamic logic circuit to work properly and causes increased leakage power and propagation delay [6].

The dynamic circuit can store capacitive voltage in the dynamic node as a memory device. These types of circuits have to change their dynamic node capacitive store voltage with the clock frequency. For that reason, these circuits are used in many fields; processors, memory, smart devices, etc. Compared to static logic circuits, dynamic circuits can function faster and use fewer transistors. But, this circuit has some limitations, like propagation delay, unwanted leakage current, etc [7] [8].

The purpose of this paper is to present a new dynamic logic circuit and technique that minimizes leakage currents and propagation delays. The remaining portions of the paper are arranged as follows: Defining the concept in Section II. In Section III, a literature study on dynamic logic circuits is covered.. Section IV analysed about proposed design. Section V contains the analysis and simulation. The conclusion part is

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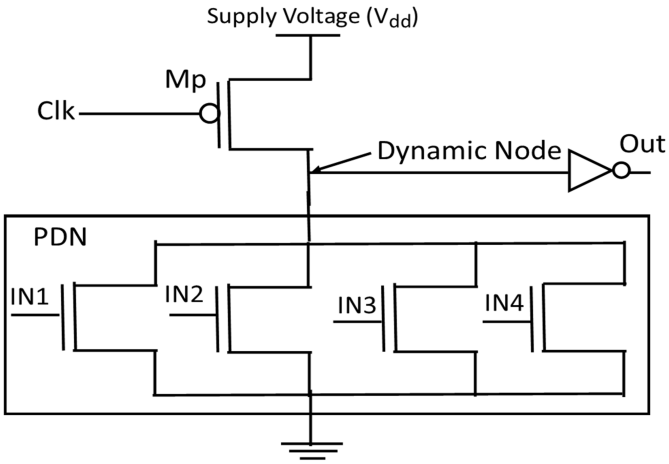

Fig. 1. Dynamic Logic Circuit Structure

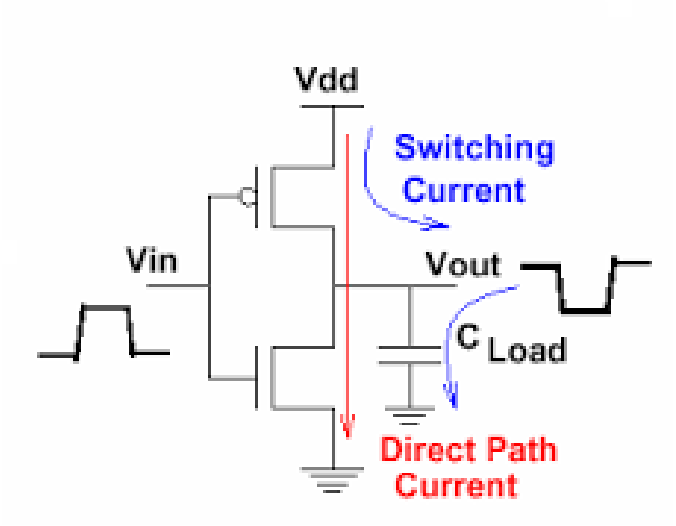

Fig. 2. CMOS Charging and Discharging Path

discussed in Section VI.

II. Clarifying The Argument

Transmission time delay is a time that occurs when an input signal goes through a transistor gate and how fast it responds to creating an inversion layer in its gate terminal. Delay is calculated using the input and output waves' 50% transition sites. Here, a clock is used from outside the circuit to control the precharge and evaluation phase in the dynamic node and the required circuit function which is indicated in Fig. 2. When clock is in logic high state the evaluation phase arrives. This period of phase is divided in two section. At first, when all the Pull down network inputs have logic zero as an input or all the inputs are turned off. The second case could be available when all the inputs of PDN are in logic high state means all are in turned on. So, when all the inputs of PDN are active during evaluation period the dynamic point can be release voltage easily with the PDN. However, During the Pull Down network transistors are inactive, the dynamic point has no way of properly discharging. In that case, dynamic node should preserve this capacitive voltage. But, this does not always happen. The subthreshold leakage in the transistors is the main problem for this stage. As a result dynamic node getting discharge through inactive PDN causing leaking current and propagation delay [9] [10] [8] [11] [6] [12].

More sub-threshold leakage current channels are produced by wide fan-in domino gates due to their increased compactness. Unwanted signal from any how enters into the input gates when PDN is off, creating a Vgs (gate to source) voltage. Discharging current and transmission time delay are also increased. This problem is denoted as the name called Crosstalk. Therefore, it is crucial to minimize transmission time delay and discharging current while constructing a dynamic circuit [13] [8] [14].

III. Previous Works

Mahmoodi et al. [3] suggested a circuit where a footed nmos is set before the ground, as represent in the Fig. 5. The propagation delay and leakage current are marginally decreased in this research. A source feeding technique called keeper is added to store the capacitive charge in dynamic point while the Pull Down Network is disabled during the assessment phase. Peiravi et al. [1] by taking consideration

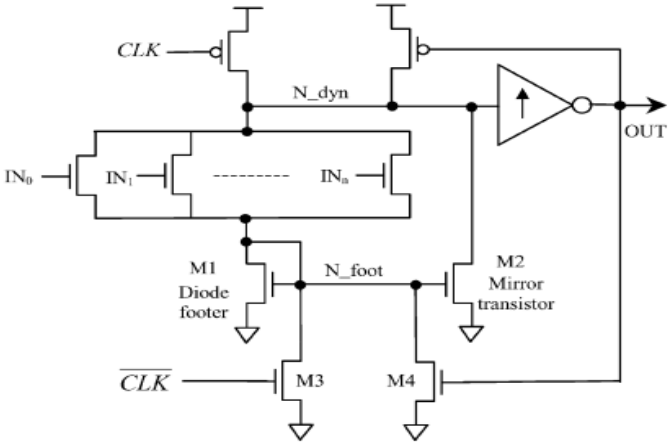

Fig. 3. Mahmudi et al. proposed model

of the discharging current for the inactive network below the dynamic point all the transistors with the switching charge of the pull down's operational transistors, a faster domino circuit method was presented for managing the PMOS feed back or feeder transistor. The stacking method also bring down discharging current and improves functionality of current mirroring circuit. kashyap et al. [15] have suggested a criteria to solve the discharging current issues. A keeper circuit is not required in order to maintain the evaluation phase's genuine

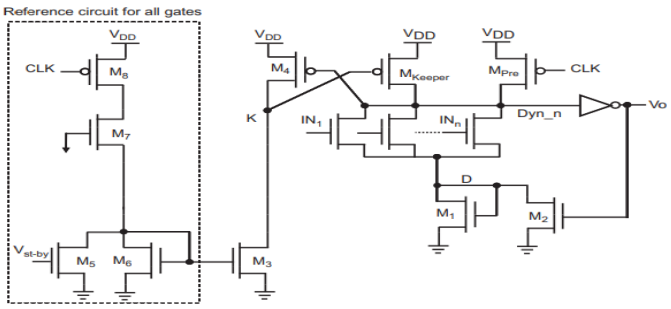

Fig. 4. Pieravi et al. proposed model

logic level. There won't be a voltage drop during the next precharge phase.

Islam et al. [16] represent a model was put forth by including a keeper controller. The gate of the keeper device is linked to the responsive waveform.

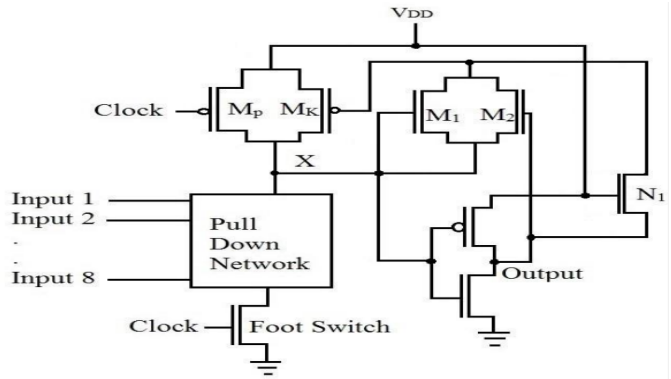

Fig. 5. Islam et al. proposed model

IV. Proposed Dynamic Logic Circuit

The four different components are added in the fundamental dynamic logic circuit in this suggested paradigm. Stacking effect, a mirror circuit, a keeper circuit, and a delay element are used to prepare proposed circuit.

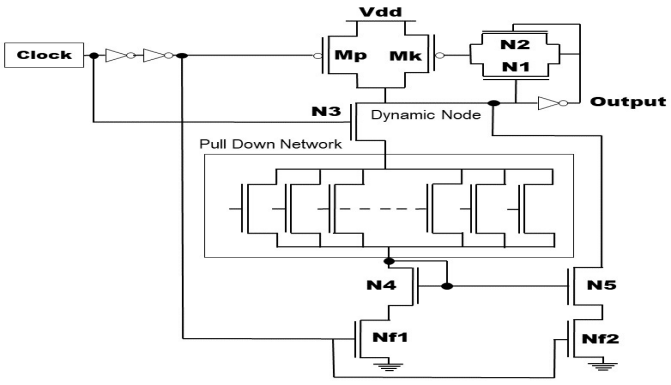

Fig. 6. Proposed Dynamic Circuit

A. Precharge Phase

A newly modified dynamic circuit is represented in Fig. 6. First, the OR logic gate operation is carried out when the network below the dynamic point is deactivated. The precharge and keeper device are turned ON at that point when the clock reaches a logic inactive state. The dynamic point will acquire a logic active state up to Vdd throughout the precharge period. The N3 transistor is still not operational. When that happens, the stacking effect circuit won't work when the clock is in a logic inactive low state. Hence, the dynamic points capacitive voltage is preserved.

B. Evaluation Phase

The clock enters the evaluation period when it is in the logic Active High. The dynamic node must push the capacitance voltage up to source voltage throughout the evaluation period. However, the PDN is not constructed with the ideal transistor because it is not activated. so that the leakage current via the PDN causes a gradual discharge of the dynamic node. Additionally, a few strategies are taken into account in sequence to control or restrict the leakage current through PDN. After the clock, the delay element is employed. This reduces leakage current during the transition time. The remaining sub-threshold leaking through the inactive pull-down network is then stopped using a N3 nmos transistor. The reduction of leakage current is not always as promising as we would want. For this, we have inserted a current mirror circuit after the pull-down network by connecting the N4 drain and gate terminal to N5 gate. Although this circuit limits the leakage current for PDN, it might not always be sufficient. For improved leakage current reduction in this circuit, we put a footer nmos at the circuit's end.

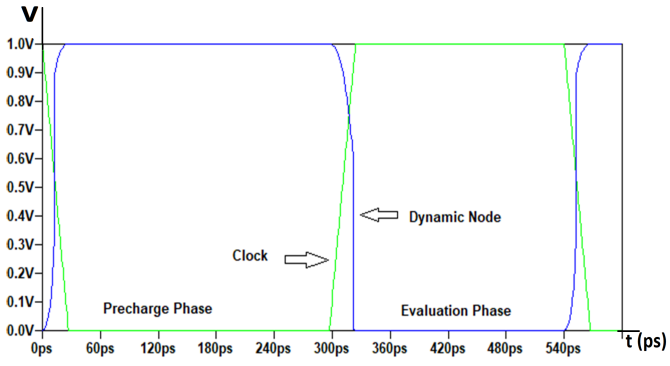

Fig. 7. Dynamic Node Simulation Waveform

Now, the pull-down network will be activated if any of its gates are set to logic high. Using the 45nm PTM technology and the LTSpice tool to design the active Pull Down Network depicted in Fig. 4, Throughout the evaluation period, a fair discharge of the dynamic point will directly connects the ground. Additionally, the stacking impact quickly lowers the Vgs voltages of NMOS in the Pull Down Network(PDN) due to noise at the PDN's gate. PDN has considered the

operation of OR-logic operation. In the suggested model, the W/L(Width-to-Lenght) ratio of NMOS is settled at 0.5. It is assumed that PMOS is wider because hole mobility in PMOS is nearly 2.7 times greater than in NMOS. The W/L(width-to-length) ratio of NMOS is set at 0.5 in the suggested model. The width of PMOS is assumed to be 2.7 times larger than that of NMOS because hole mobility is almost 2.7 times slower than electron mobility [17].

V. Simulation Result and Analysis

In Fig. 7, the simulation waveform of the dynamic node is presented for 16-input OR gate circuit in PDN.

TABLE I. Propagation delay compare to prior models for 16-bit OR logic operation with a source voltage 0.7V

Compared Models	Delay (ps)
Proposed	16.5
MM Kabir et al. [8]	17.1
HSD [1]	17.91
kashyap et al. [15]	22.38
Footer Dynamic Logic [3]	32.41

TABLE II. Leakage current compare to prior models for 16-bit OR logic operation with a source voltage 0.7V

Different Models	Leakage Current (nA)
Proposed	131
MM Kabir et al. [8]	174
Islam et al. [16]	211
Footer Dynamic Logic [3]	346
kashyap et al. [15]	352
F Abrar et al. [11]	435

Table I compares propagation delays with the proposed model to earlier recommended models for the 16-bit OR logic operation with a source voltage of 0.7V. The new model has a promising minimal latency when compared to the previous model's other dynamic circuit. Table II compares the leakage currents of alternative models for the 16-bit OR logic operation with the proposed model leakage current for the 16-bit OR logic operation with a source voltage of 0.7V. It has the lowest leakage current compared to prior models.

The comparative examination of the transmission time delay of the suggested method with variations in threshold voltage with a source voltage of 0.7V for 16-bit OR logic operation is shown in Fig. 8. The propagation delay increases when the threshold voltage increases somewhat in this picture, and vice versa. As a result, in the suggested model, latency changes linearly with the change in threshold voltage. Leakage current varies with threshold voltage, as demonstrated in Fig. 9. In this scenario, the proposed model exhibits an equivalent relationship: increasing the threshold voltage decreases leakage current and vice versa. In contrast, Fig. 10 depicts the comparative relationship between W/L ratio and delay for 16-input OR gate operation with a 0.7V source voltage.

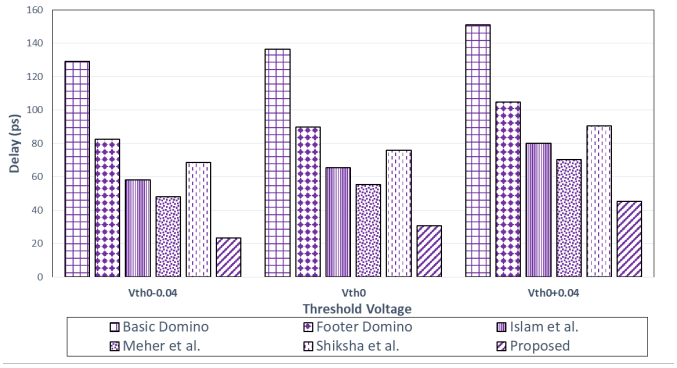

Fig. 8. Relation between delay with supply voltage of 0.7V for 16-input OR gate circuit

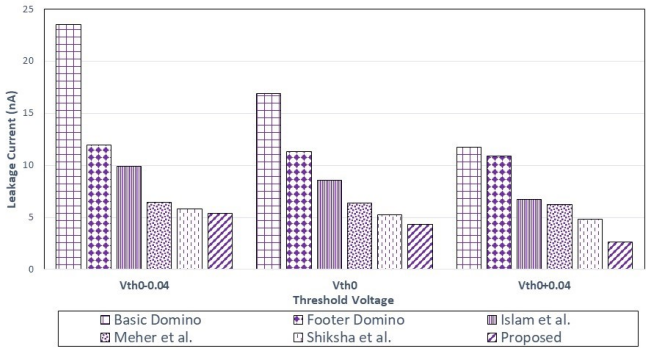

Fig. 9. Relative changes in the leakage current with various threshold in gate as input for 16-input OR gate circuit

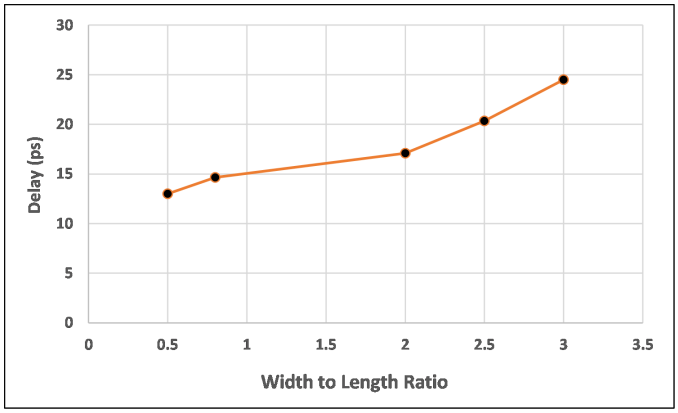

Fig. 10. Comparative relation between delay with threshold voltage at supply voltage 0.7V (16-bit OR logic operation)

VI. Conclusion

This study proposes a novel method for constructing dynamic logic circuits that can withstand leakage current and propagation delay. The delay circuit, keeper hold circuit, stacking nmos, and mirror circuit concepts are mainly used to achieve our purpose. The right width to length ratio scaling of the transistors in the suggested method can significantly improve output performance. For the proposed model, the OR-logic operation is explored. This proposed model can also make use of any of the other logic operations. The Spice predictive technology model for 45nm LTSpice software is used to simulate this proposed model. In comparison to others, the prefer model satisfies in terms of promised discharging current and limiting the transmission time delay. As a result, this model appears to be promising for developing low discharging current and transmission time delay-required applications.

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